AMENDMENTS TO THE CLAIMS

1. (Currently amended) An apparatus for controlling a bank refresh including a plurality of banks, comprising:

a plurality of input buffer means for buffering bank address signals inputted from an external circuit with the command signal;

a reset control unit for receiving output signals from the plurality of input buffer means to thereby generate a reset signal;

a counter for producing count signals wherein the counter is reset by the reset signal, ~~being reset by an output signals from the plurality of input buffer means~~;

a switch means for combining the count signals from the counter in order to produce internal bank refresh signals in response to bank address signals from the plurality of input buffer means; and

a chipset control means for generating a plurality of internal bank addresses for the refresh using the internal bank refresh signals,

~~wherein each input buffer means includes a latch means for sustaining the output signals of the plurality of input buffer means within a certain period of time only when the refresh command signals are applied~~

wherein the reset control unit includes a NOR gate for combining the output signals from the plurality of input buffer means.

2. (Previously presented) The apparatus as recited in claim 1, wherein the number of the plurality of input buffer means is N and the counter is (N-1)-nary, if the number of the plurality of banks is 2^N.

3. (Cancelled).

4. (Original) The apparatus as recited in claim 2, wherein the (N-1)-nary counter is reset by a logic combination of the bank address signals.

5. (Currently amended) A method for controlling a bank refresh including 2^N of banks, comprising the steps of:

a) buffering N bank address signals inputted from the external circuit with the refresh command signals;

b) generating a reset signal based on the logic NOR operation of the N buffered bank address signals;

~~b~~c) outputting the (N-1)-nary count signal in sequence by ~~resetting at least one of N buffered signals~~ inputting the reset signal;

~~e~~d) switching and outputting unit of N-1 count signals to the bank refresh combination signals in response to the N buffered signals; and

~~d~~e) generating an internal bank address for the refresh using the bank refresh combination signals.

6. (Previously presented) The apparatus as recited in claim 4, wherein N is at least three.

7. (Currently amended) The ~~apparatus as recited in~~ method of claim 5, wherein N is a positive integer and N is at least three.

8. (New) The apparatus as recited in claim 1, wherein each input buffer means includes a latch means for sustaining the output signals of the plurality of input buffer means within a certain period of time only when the refresh command signals are applied.

9. (New) The apparatus as recited in claim 1, wherein the reset control unit further includes a inverter for inverting an output signal from the NOR gate.